IN THE ABSTRACT OF THE DISCLOSURE

Please amend the Abstract as follows:

The present invention relates to a power socket for a microelectronic device that, in one embodiment, uses a low-resistance power and ground terminal configuration. In another embodiment, a low-resistance power and ground terminal configuration is combined on the power socket with a vertically oriented interdigital capacitor that is used to lower inductance. By this combination a significantly lowered impedance is achieved during operation of the microelectronic device. The capacitor may include plates that are vertically oriented relative to the major planar surface of the socket faces and capacitors may be located between a power and a ground contact, between two power contacts, or between two ground contacts.